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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,369	03/11/2004	Hilario L. Oh	6601P074	8868

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EXAMINER	
PHAM, THOMAS K	

ART UNIT	PAPER NUMBER
2121	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/800,369	OH, HILARIO L.	
	Examiner	Art Unit	
	Thomas K. Pham	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

First Action on the Merits

1. Claims 1-20 of U.S. Application 10/800,369 filed on 03/11/2004 are presented for examination.

Quotations of U.S. Code Title 35

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim Rejections - 35 USC § 103

6. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,707,545 ("Hunter") in view of U.S. Patent No. 4,850,027 ("Kimmel").

Regarding claim 1

Hunter teaches in a semiconductor wafer fabrication system that includes at least a track system and a scanner system, a method of compensating the fabrication system for deviations from nominal scanner system clock periodicity, the method comprising the steps: operating said scanner system (see Col. 6 lines 48-65, Col. 7 lines 11-20 and Col. 10 lines 39-46); operating said track system (see Col. 5 lines 52-59 and Col. 8 lines 7-22).

Hunter does not specifically teach the method comprising the steps: the scanner is responsive to a signal from a scanner system clock; the track system responsive to a signal from a track system clock; pre-determining and inserting wait states as needed to avoid conflict for resources in said semiconductor wafer fabrication system; and determining deviation from nominal timing in said scanner clock and dynamically inserting time delay as needed in said semiconductor wafer fabrication system to compensate for such deviation.

However, Kimmel teaches parallel pipeline image processing system for compensating the delay time for processing image streams (see Col. 11 lines 17-35) comprising processing elements that responsive to signal from a system clock (see Col. 11 lines 31-37); pre-determining and dynamically inserting delay time as needed to avoid conflict between different path of processing (see Col. 11 lines 51-63) for the purpose of keeping everything in synchronization regardless of any path the images may taken which could cause additional image processing delay (see Col. 15 lines 21-28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the compensating method of Kimmel with the system of Hunter because it would provide for the purpose of keeping everything in synchronization regardless of any path the images may taken which could cause additional image processing delay.

Regarding claim 10

Hunter teaches a semiconductor wafer fabrication system, comprising: a scanner system (see Col. 7 lines 11-20); a track system (see Col. 5 lines 52-59); means for moving at least one wafer within said semiconductor wafer fabrication system (see Col. 8 lines 7-22).

Hunter does not specifically teach the scanner is responsive to a signal from a scanner system clock; the track system responsive to a signal from a track system clock; means for inserting pre-planned wait states in said single-clock semiconductor wafer fabrication system to reduce conflict for resources in said semiconductor wafer fabrication system; and means for dynamically inserting time delay as needed in said semiconductor wafer fabrication system to compensate for disturbance in periodicity of said scanner clock.

However, Kimmel teaches parallel pipeline image processing system for compensating the delay time for processing image streams (see Col. 11 lines 17-35) comprising processing elements (PE) that responsive to signal from a system clock (see Col. 11 lines 31-37); dynamically inserting delay time as needed to avoid conflict between different path of processing (see Col. 11 lines 51-63) for the purpose of keeping everything in synchronization regardless of any path the images may taken which could cause additional image processing delay (see Col. 15 lines 21-28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the compensating method of Kimmel with the system of Hunter because it would provide for the purpose of keeping everything in synchronization regardless of any path the images may taken which could cause additional image processing delay.

Regarding claim 18

Hunter teaches for use in operating a semiconductor wafer fabrication system that includes at least a scanner system (see Col. 7 lines 11-20), and a track system (see Col. 5 lines 52-59). Hunter does not specifically teach the scanner is responsive to a signal from a scanner system clock; the track system responsive to a signal from a track system clock, and a computer readable medium storing a computer program that when executed carries out at least one of the following steps: determines deviations from nominal periodicity in said scanner system clock; and calculates and dynamically inserts time delay as needed in said semiconductor wafer fabrication system to compensate for said deviations.

However, Kimmel teaches parallel pipeline image processing system for compensating the delay time for processing image streams (see Col. 11 lines 17-35) comprising processing elements (PE) that responsive to signal from a system clock (see Col. 11 lines 31-37); dynamically inserting delay time as needed to avoid conflict between different path of processing (see Col. 11 lines 51-63) for the purpose of keeping everything in synchronization regardless of any path the images may taken which could cause additional image processing delay (see Col. 15 lines 21-28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the compensating method of Kimmel with the system of Hunter because

it would provide for the purpose of keeping everything in synchronization regardless of any path the images may taken which could cause additional image processing delay.

Regarding claims 2, 3, 11 and 12

Hunter teaches the throughput of the wafers is monitored by determining when a given substrate enters and exits the processing system, where data collected can be used to determine peak and average throughput.

It should be noted that the number of wafers per hour throughput for the system is given very little patentable weight. In the absence of any new or unexpected results, the number of wafers per hour throughput are considered to be set to any values operate on a specific device.

Regarding claims 4 and 13

Kimmel teaches location and length of each said time wait is determined by a computer system controlling (see Col. 7 lines 20-29).

Regarding claim 5

Hunter teaches semiconductor wafer fabrication system includes at least two robotic stations (see FIG. 1A).

Regarding claim 6

Hunter teaches semiconductor wafer fabrication system includes at least three robotic stations (see FIG. 1A).

Regarding claim 7

Hunter teaches said semiconductor wafer fabrication system includes at least four robotic stations (see FIG. 1A).

Regarding claim 8

Kimmel teaches the pre-determining, dynamically inserting and determining deviation are carried out by a computer system (see Col. 7 lines 20-29).

Regarding claim 9

Kimmel teaches said track system operates responsive to a signal from said track system clock, and said scanner system operates responsive to a signal from said scanner system clock (see Col. 11 lines 31-37).

Regarding claim 14

Kimmel teaches means for dynamically inserting time delay includes a computer system (see Col. 11 lines 51-63).

Regarding claim 15

Kimmel teaches said computer system generates at least said scanner system clock (see Col. 7 lines 20-29).

Regarding claim 16

Hunter teaches means for moving includes at least two robotic stations (see FIG. 1A).

Regarding claim 17

Hunter teaches means for moving includes at least three robotic stations (see FIG. 1A).

Regarding claim 19

Kimmel teaches wherein said program when executed statically determines pre-planned wait states to minimize resource conflict within said semiconductor wafer production system (see Col. 11 lines 22-28).

Regarding claim 20

Kimmel teaches wherein said program when executed dynamically determines deviations from nominal periodicity in said scanner system clock, and calculates time delay needed to compensate for said deviations (see Col. 11 lines 51-63).

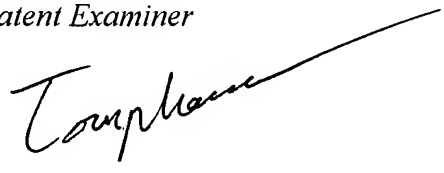
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner *Thomas Pham*; whose telephone number is (571) 272-3689, Monday - Thursday from 6:30 AM - 5:00 PM EST or contact Supervisor *Mr. Anthony Knight* at (571) 272-3687.

Any response to this office action should be mailed to: **Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.** Responses may also be faxed to the **official fax number (571) 273-8300.**

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas Pham
Patent Examiner



February 9, 2006